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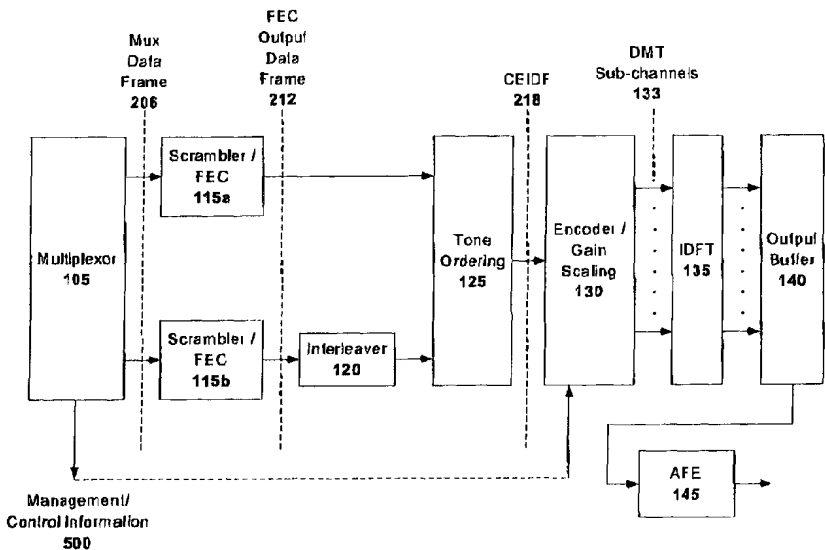
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(54) Title: OPTIMUM OVERHEAD FRAMING TECHNIQUES FOR ADSL DMT MODEMS



(57) Abstract: Techniques described herein can be used at least by transceiver systems based on G.992.1 and G.992.2 to allocate management/control information for transmission using DMT symbols. In one embodiment of the present invention, a separate management/control information channel is allocated independent of interleaved and fast paths. Advantageously, if management and overhead information need to be transmitted quickly or often, valuable data payload bandwidth of the fast path is not used and the slow transmission of the interleaved path is avoided. In another embodiment of the present invention, a management/control information channel may be allocated independent of interleaved and fast paths, but distinct path specific sync bytes may be allocated to one or both of the interleaved and fast paths to carry path specific information.

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OPTIMUM OVERHEAD FRAMING TECHNIQUES FOR ADSL DMT MODEMS

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. Provisional Patent Application Serial No. 60/240,001 filed October 12, 2000, U.S. Provisional Patent Application Serial No. 60/239,398 filed October 5, 2000, and U.S. Provisional Patent Application Serial No. 60/235,150 filed September 22, 2000, which are all incorporated by reference in their entirety.

15 FIELD OF THE INVENTION

[0002] The present invention relates generally to the field of communications systems and more specifically to overhead information multiplexing in asymmetric digital subscriber line modems.

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RELATED ART

[0003] The Telecommunications Standards Section of the International Telecommunication Union (ITU-T) develops recommendations to facilitate the interoperation of telecommunication networks. Two of these recommendations are designated as G.992.1 (sometimes referred to as G.dmt) and G.992.2 (sometimes referred to as G.lite), both of which are incorporated herein by reference in their entirety. Recommendation G.992.1 refers to an asymmetric digital subscriber line (ADSL) transceiver that is an ADSL industry standard for typical network access at data rates up to 8.192 Mbit/s downstream and 640 kbit/s upstream. Recommendation G.992.2, on the other hand, refers to an ADSL transceiver that is a lower data rate version of a G.992.1 ADSL transceiver. Data rates up to 1.5 Mbit/s in the downstream direction and 512 kbit/s upstream are typical with this standard. Factors such as the electrical characteristics of the customer's equipment, the distance between the subscriber and central office, and the error rate allowed all contribute to the data rate of G992.1 and G992.2 transceivers. For example, Figure 1A depicts a pair of ADSL transceivers between a network operator end (ATU-C) and a customer end (ATU-R) in, for example, G.992.1 and G.992.2 compliant systems.

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5 [0004] G.992.1 and G.992.2 transceivers both employ discrete multi-tone (DMT) technology. DMT is a form of multicarrier modulation in which the spectrum of the input signal is spread over numerous bands, also referred to as sub-channels. Each sub-channel is modulated to some carrier frequency. By working with a large number of carriers rather than a single carrier, the available channel capacity is maximized thereby optimizing performance of the transmission. A DMT symbol is the basic unit of information transmitted by an ADSL transceiver.

10 [0005] Both G.992.1 and G.992.2 further describe a DMT ADSL system data framing that is designed to provide a fixed overhead per DMT symbol. Overhead includes information about the transceiver pair and performance management. Consequently, G.992.1 and G.992.2 allocate a fixed bandwidth for overhead. One drawback with fixed overhead bandwidth is that bandwidth which could have been used for data transfer is allocated for overhead, even if the entire allocated overhead bandwidth is not used. In cases
15 where the overhead bandwidth is transmitted using an "interleaved" or "slow" path, overhead information may not be transferred quickly enough. Further, in some implementations of G.992.1 and G.992, overhead bytes are allocated for various types of transmissions and so, when more overhead bandwidth is needed for a specific type of overhead transmission, that bandwidth is not available.

20 [0006] What is needed, therefore, are optimum overhead framing techniques for ADSL modems that minimize the use of bandwidth used for overhead information transfer and provide flexibility to repartition the bandwidth available to overhead information, among specific portions of overhead information.

25 SUMMARY

30 [0007] One embodiment of the present invention includes a method of allocating overhead within DMT ADSL frames, where the method includes allocating an interleaved data path; allocating a fast data path; allocating a path for overhead and management information independent of the fast and interleaved data paths; and within a DMT ADSL frame, combining the overhead and management information with the interleaved and fast data paths.

35 [0008] One embodiment of the present invention includes a method of allocating overhead within DMT ADSL frames, where the method includes: allocating an interleaved data path; allocating first sync bytes among the interleaved data path; allocating a fast data path; allocating second sync bytes among the fast data path; allocating a path for overhead

and management information independent of the fast and interleaved data paths; and within a DMT ADSL frame, combining the overhead and management information with the interleaved and fast data paths.

- 5 [0009] Advantageously, a dedicated overhead and management information channel is provided so that if management and overhead information needs to be transmitted quickly or often, valuable data payload bandwidth of the fast path is not used and the slow transmission of the interleaved path is avoided.
- 10 [0010] Various embodiments of the present invention will be more fully understood in light of the following detailed description taken together with the accompanying drawings. It should be noted that the language used in the specification has been principally selected for readability and instructional purposes and not to limit the scope of the inventive subject matter.

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BRIEF DESCRIPTION OF THE DRAWINGS

- [0011] Figure 1A depicts a pair of ADSL transceivers.
- [0012] Figure 1B is a block diagram of an ADSL transmitter that may be configured in accordance with embodiments of the present invention.
- 20 [0013] Figure 2A depicts a suitable overhead byte and field allocations used in techniques to allocate management/control information for transmission using DMT symbols in accordance with an embodiment of the present invention.
- [0014] Figure 2B depicts suitable overhead byte and field allocations used in techniques to allocate management/control information for transmission using DMT symbols in
- 25 accordance with another embodiment of the present invention.
- [0015] Figure 3A depicts a format of a management/control information block 500A in accordance with another embodiment of the present invention.
- [0016] Figure 3B depicts a format of a management/control information block 500B in accordance with another embodiment of the present invention.
- 30 [0017] Figure 3C depicts a format of a management/control information block 500C in accordance with another embodiment of the present invention.
- [0018] Figure 4 depicts a process for dynamically allocating the available overhead bytes in accordance with an embodiment of the present invention.

[0019] Note that use of the same reference numbers in different figures indicates the same or like elements.

DETAILED DESCRIPTION

5 **[0020]** Figure 1B is a block diagram of an ADSL transmitter that may be configured in accordance with embodiments of the present invention described with respect to Figures 2A and 2B and Figures 3A-3C. Figure 1B merely illustrates an example of an ADSL transmitter and can be replaced with other ADSL transmitters. For example, other
10 embodiments of the transmitter may include modules not shown in the figure (e.g., an amplifier, line driver, anti-aliasing filter, and hybrid circuitry). Likewise, other embodiments of the transmitter may not include some of the modules shown (e.g., FEC module or interleaving module) on one of the latency paths. The transmitter components may be implemented in hardware, software, firmware or any combination thereof. For
15 example, each of the components shown in Figure 1B may be implemented as one or more application specific integrated circuits. Likewise, the components may be implemented as a set (or sets) of instructions running on one or more digital signal processors. Numerous embodiments and configurations will be apparent in light of this disclosure. For example, a suitable embodiment of the transmitter of Figure 1B is described in U.S. Patent Application No. 09/846,883, entitled "FRAMING TECHNIQUES FOR ADSL SYSTEMS", filed May 1, 2001,
20 which is incorporated herein by reference in its entirety.

[0021] The transmitter of Figure 1B includes a multiplexor module 105, scrambler and forward error correction (FEC) modules 115a and 115b, an interleaver module 120, a tone ordering module 125, an encoder and gain scaling module 130, an inverse discrete Fourier
25 transform (IDFT) module 135, a output buffer 140, and an analog front end 145. Generally, the transmitter illustrated is based on a model for facilitating understanding of transmitter function in accordance with ITU Recommendations G.992.1 and G.992.2 (collectively referred to as ADSL standards).

30 **[0022]** The transmitter shown in Figure 1B may be deployed in either the upstream or downstream direction. The multiplexor module 105 multiplexes requisite overhead (e.g., CRC bits, indicator bits, eoc and aoc messages are carried over what is commonly referred to as a sync byte) with the user payload data from a system interface (e.g., ATM or STM). Typically, there are two latency paths in the transmitter (e.g., a fast path and an interleaved
35 path). Note, however, that alternative embodiments may include more than two latency paths. Additional paths may optionally include either or both an FEC module and an interleaver module. In general, a fast latency path (e.g., including scrambler/FEC module

115a) may be configured to provide lower latency than an interleaved path. An interleaved path (e.g., including scrambler/FEC module 115b and interleaver module 120), on the other hand, provides protection against burst errors due to the transmitted signal clipping or impulse noise at the cost of greater latency.

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[0023] In the embodiment shown, the mux data frames provided by multiplexor 105 to each latency path are subjected to scrambling and forward error correction coding (e.g., 115a and b). In addition, the mux data frames provided by multiplexor 105 to the interleaved latency path are subjected to an interleaver function (e.g., 120). The two data streams may then be combined into a data symbol that is input to the constellation encoder (e.g., 130). Before a data symbol is mapped to the sub-carrier constellations, the sub-carriers may be appropriately tone ordered (e.g., 125). After constellation encoding, the data is modulated (e.g., 135), buffered (e.g., 140), and converted (e.g., 145) to its analog equivalent to facilitate transmission across the transmission loop.

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[0024] Because of the addition of FEC redundancy bytes and data interleaving, the various intermediate data frames (bit-level data prior to constellation encoding) have different structure at three reference points of the transmitter. These reference points are shown in Figure 1B and include 206 (mux data frame), 212 (FEC output data frame), and 218 (constellation encoder input data frame). Generally, the present invention provides a framing technique and framing parameters that result in a certain order of sync, payload data and the RS codeword redundancy bytes to achieve programmable fixed overhead efficient framing that allows seamless rate changes.

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Components

[0025] The multiplexor module 105 multiplexes the user payload data bytes and overhead bytes (e.g., sync bytes). The multiplexor module 105 may include, for example, a multiplexor for each latency path and separate buffers (e.g., a fast buffer and an interleaved buffer) to store the multiplexed data for each corresponding latency path. In the embodiment shown, the multiplexor on each of the latency paths (whether downstream or upstream) has a mux data frame rate that is either synchronized to a 4 kbps ADSL DMT symbol rate or to its known fraction or a multiple through a multiplying factor.

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[0026] In the embodiment shown, a cyclic redundancy check (CRC) is performed on the multiplexed data for each latency path. Generally, the CRC bits of a particular latency path are carried in a sync byte included in each mux data frame assigned to that latency path after every 68 DMT symbols. Remaining sync bytes that are transmitted over 68 DMT symbols

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(e.g., an ADSL superframe) carry other overhead related information (e.g., indicator bits, eoc and aoc messages). The multiplexor module 105 outputs mux data frames 206.

5 **[0027]** For the sake of clarity, note that current ADSL standards define a superframe structure. Each superframe is composed of a number of data frames (e.g., 68 data frames numbered 0 through 67). These data frames are encoded and modulated into DMT symbols. Each DMT symbol is followed by a synchronization symbol. In general, such synchronization symbols carry no user or overhead bit-level data and are inserted by the modulator (e.g., 135) to establish superframe boundaries. From the bit-level and user data
10 perspective, the DMT symbol rate is 4000 baud resulting in a period equal to .25 milliseconds (in accordance with ADSL standards). However, in order to allow for the insertion of the synchronization symbol, the actual transmitted DMT symbol rate is $69/68$ times 4,000 baud.

15 **[0028]** In the scrambler and FEC modules 115a and 115b, the scrambler (e.g. when present and operational) operates on the output data buffer of each mux data frame 206 in order to randomize the data pattern as is conventionally done. Such randomizing is for optimizing the transmission performance. Scrambling also minimizes the possibility of repetitive data patterns. Generally, FEC is based on Reed-Solomon (RS) coding. The size
20 (in bytes) of a resulting RS codeword is $N_{FEC} = K + R$, where the number of check bytes R and codeword size N_{FEC} vary depending on the number of bits assigned to each latency path and the latency requirements associated with each path. The scrambler and FEC modules 115 output the RS codewords, which form the FEC output data frames 212.

25 **[0029]** The interleaver module 120 performs a conventional interleaving function on the FEC output data frames 212. In one embodiment, the FEC output data frames 212 are convolutionally interleaved in accordance with ADSL standards to a specified interleave depth. Generally, the interleaving process delays each byte of a given FEC output data
30 frame 212 by a different amount. This results in the constellation encoder input data frames 218 containing bytes from a number of different FEC output data frames 212. Given a convolutional interleaving algorithm and the interleaving depths (e.g., powers of 2), the output bytes from the interleaver always occupy distinct time slots when the RS codeword size (N) is odd. When N is an even number of bytes, a dummy byte can be added at the beginning of the RS codeword at the input to the interleaver. The resultant odd-length RS
35 codeword is then convolutionally interleaved. The dummy byte is then removed from the output of the interleaver.

5 **[0030]** The tone ordering module 125 provides a tone ordering algorithm (e.g., vendor specified) to reduce the errors related to clipping caused by the digital-to-analog converter (not shown) of the transmitter. In general, the numbers of bits and the relative gains to be used for every tone are predetermined by the receiver (e.g., by conventional bitloading assignment techniques) and provided to the transmitter. These bit-gain pairs are typically stored in ascending order of frequency (e.g., as designated by tone number) in a bit and gain table. “Tone-ordered” encoding can then be performed, where bits from a fast path are assigned to the tones with the smallest bit assignment, and bits from an interleaved path are assigned to the remaining tones. As is known in the art and illustrated in ADSL standards, 10 tone ordering and bit extraction may be performed with and without trellis coding. Note that because the data from the fast path is not interleaved, the constellation encoder input data frame 218 is identical to the corresponding FEC output data frame 212 (if fast path is the only latency path used).

15 **[0031]** The encoder and gain scaling module 130, which can be implemented with or without trellis coding, receives the constellation encoder input data frames 218 and encodes them as signal points in signal constellations based on a given tone ordering. The encoder and gain scaling module 130 may further include a convolutional encoder module for obtaining the coding gain. In one embodiment, for each sub-channel, QAM modulation is used where each constellation signal point has an in-phase component and a quadrature component. Depending on the constellation size of each DMT sub-channel, each sub-carrier carries multiple bits. For example, 64-QAM has 64 points in the constellation. This means that a sub-channel can carry six binary bits. A larger constellation size carries more bits per symbol. Sub-channels can have different constellation sizes. The total number of 20 bits transmitted is the sum of the number of bits transmitted by each sub-channel. A number of sub-channels 133 (e.g., 255 for downstream, 31 for upstream with appropriate gain scaling) are provided by the encoder and gain scaling module 130 to the IDFT module 135.

30 **[0032]** The inverse discrete Fourier transform (IDFT) module 135 modulates the constellations (e.g., QAM constellations) output by the encoder and gain scaling module 130 on to the available transmission DMT sub-channels and combines all the sub-channels together for transmission. The output buffer 140 stores the modulated samples for transmission. The analog front end (AFE) 145 converts the samples to analog signals, 35 which are then filtered, amplified and coupled to the transmission line. Note that the IDFT module 135, the output buffer 140 and the analog front end 145 may be implemented in conventional technology.

Overhead Channel Management

[0033] Embodiments of the present invention described herein can be used at least by transceiver systems based on G.992.1 and G.992.2 to allocate management and control information for transmission using DMT symbols. Figures 2A and 2B depict suitable overhead byte and field allocations used to allocate management/control information for transmission using DMT symbols in accordance with embodiments of the present invention. The examples provided in Figures 2A and 2B show outputs by each of multiplexor 105, module 115a, module 115b, the interleaver 120, tone ordering module 125, and the transmitter of Figure 1B (as DMT symbols). Overhead byte allocations in accordance with examples provided in Figures 2A, 2B and Figures 3A-3C may be suitably implemented by using the transmitter described with respect to Figure 1B (or another transmitter) in combination with software instructions executed by a digital signal processing device or other central processing unit, firmware, and/or hardware.

Figure 2A

[0034] Figure 2A depicts suitable overhead byte and field allocations used in techniques to allocate management/control information for transmission using DMT symbols in accordance with an embodiment of the present invention. In Figure 2A, framer bearer channels 434 are input into multiplexor 105. Framer bearer channels 434 include, for example, data, voice, and video. Multiplexor 105 outputs framer bearer channels 436 to module 115a (“fast path”) and outputs framer bearer channels 442 to module 115b (“interleaved path”). Module 115a allocates respective framer bearer channels 436 into respective FEC output data frames 437. The tones to be transmitted are ordered by module 125. Module 115a transfers the FEC output data frames 437 to the encoder gain scaling module 130. Module 115b allocates respective framer bearer channels 442 into respective FEC output data frames 443. Interleaver 120 (Figure 1B) is coupled to receive the FEC output data frames 443 from module 115b. Interleaver 120 interleaves FEC output data frames 443 from module 115b in a manner described earlier and outputs the interleaved FEC output data frames 443 to the encoder gain scaling module 130.

[0035] Management protocol specific transmission-convergence (MPS-TC) framer bytes are input into multiplexor 105. For example, MPS-TC includes conventional information such as eoc, aoc, loss of signal, remote defect indicator, and network timing reference signals as described in G.992.1 and G.992.2. Multiplexed bytes of the MPS-TC framer bytes (hereafter “management/control information 500”) are output from the multiplexor 105 and input into encoder/gain scaling 130. Figures 3A-3C depict example

embodiments of the management/control information 500. Advantageously, in this embodiment, no sync bytes or overhead information are allocated for either of the interleaved or fast paths. Rather management and overhead information are reserved for transmission using the management/control information 500. Advantageously, if management and overhead information needs to be transmitted quickly or often, valuable data payload bandwidth of the fast path is not used and the slow transmission of the interleaved path is avoided. As described in more detail with respect to Figure 3B, the contents of the management/control information path can be modified thereby to provide flexible rate repartitioning of certain types of management/control information.

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[0036] The transmitter allocates among DMT symbols the following: L_S bits of management/control information 500, L_0 bits of the mux data frames (MDF) from the fast path (e.g., module 115a), and L_1 bits of the FEC output data frames from the slow path (e.g., module 115b). Values L_S , L_0 and L_1 are determined based on available bandwidth of the channel, and desired partitioning of this bandwidth between different latency paths.

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Figure 2B

[0037] Figure 2B depicts suitable overhead byte and field allocations used in techniques to allocate management/control information for transmission using DMT symbols in accordance with an embodiment of the present invention. The embodiment of Figure 2B is similar to that of Figure 2A except that the interleaved and fast paths also transmit sync bytes thereby to transmit some of the overhead and management information suitable for transmission on these paths. One example of such overhead information is the latency path CRC information. Although it can also be sent as in Figure 2A, sending sync bytes in the fast and interleaved paths may provide some implementation ease because, for example, fewer gates and control logic are needed.

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[0038] In Figure 2B, framer bearer channels 450 are input into multiplexor 105. Framer bearer channels 450 include, for example, data, voice, and video as well as channel management and overhead information. Multiplexor 105 transfers frames 454 and 456 to respective modules 115a and 115b. Modules 115a and 115b process respective fast and interleaved paths. In this embodiment, fast and interleaved paths include overhead and management information, which are depicted in Figure 2B as respective Ns_0 sync bytes 452 and Ns_1 sync bytes 458. In this embodiment, sync bytes include path specific (e.g., fast or interleaved) information such as CRC over data path, FEC and ATM cells related information, if applicable.

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[0039] Module 115a allocates frame 454 with Ns0 sync bytes 452 into FEC output data frames 460. The tones to be transmitted are ordered by module 125. Module 115a outputs the FEC output data frames 460 to the encoder/gain scaling module 130. Module 115b allocates frame 456 with Ns1 sync bytes 458 into FEC output data frames 462. Interleaver 120 is coupled to receive the FEC output data frames 462 from module 115b. Interleaver 120 interleaves FEC output data frames 462 from module 115b and outputs the interleaved FEC output data frames 462 to the encoder/gain scaling module 130.

Figure 3A

[0040] Figure 3A depicts a format of a management/control information 500 in block 500A. In accordance with an embodiment of the present invention, block 500A includes fields 502, 504 and 506. Field 502 may include latency path related CRC bytes. Field 504 may include indicator bit (IB) bytes. Field 506 may include aoc, eoc, voice signaling bytes, which are encapsulated and multiplexed in an HDLC (High Level Data Link Control) frame. Fields 502, 504, and 506 are multiplexed by multiplexor 105 into block 500A. Block 500A can be 68 bytes although the number of bytes can be varied. The length of the block 500A can be determined so that the rate of transfer of block 500A is as desired. The length of block 500A can also be set to be long enough to be spread evenly over 68 DMT symbols.

[0041] The number of bytes of fields 502 to 506 within block 500A may be fixed by the network administrator and communicated by and among the transmitter and receiver pairs such as that depicted in Figure 1A. Exact positions of bytes of fields 502 to 506 within block 500A may be arbitrary.

Figure 3B

[0042] Figure 3B depicts a format of a management/control information block 500 in block 500B. In accordance with an embodiment of the present invention, block 500B includes fields 508, 510, 512, and 514. Field 508 may include latency paths related CRC bytes. Field 510 may include IB bytes. Field 512 may include aoc and eoc bytes encapsulated in an HDLC frame (hereafter HDLC1). Field 514 may include voice signaling bytes also encapsulated in a separate HDLC frame (hereafter HDLC2). Fields 508, 510, 512, and 514 are multiplexed by multiplexor 105 into block 500B.

[0043] In one embodiment, block 500B is 68 bytes long. The length of block 500B can be set so to be long enough to be spread evenly over 68 DMT symbols. The number of

bytes within block 500B is represented by $N_{500B} = N_{CRC} + N_{IB} + N_{HDLC1} + N_{HDLC2}$. In this embodiment, the number of CRC and IB bytes allocated within overhead information block are fixed based on number of latency paths. However, the number of bytes occupied by HDLC1 and HDLC2 within the overhead information block are dynamically allocable using the process described with respect to Figure 4. The positions of the contents of fields 508, 510, 512, and 514 within block 500B are arbitrary.

Figure 3C

[0044] Figure 3C depicts a format of a management/control information block 500C in accordance with another embodiment of the present invention. Block 500C may include fields 518 and 520. Field 518 may include IB bytes whereas field 520 may include aoc, eoc and voice signaling bytes encapsulated in an HDLC frame. Fields 518 and 520 are multiplexed by multiplexor 105 into block 500C.

[0045] In one embodiment, block 500C is 68 bytes long. The length of block 500C can be set so to be long enough to be spread evenly over 68 DMT symbols. In this embodiment, the number of bytes of fields 518 and 520 are fixed. The positions of the contents of fields 518 and 520 within block 500C are arbitrary.

Figure 4

[0046] Figure 4 depicts a process for dynamically allocating the number of bytes available to the combination of HDLC1 and HDLC2 in the case of block 500B of Figure 3B in accordance with an embodiment of the present invention. This process may be implemented by using the transmitter described with respect to Figure 1B (or another transmitter) in combination with software instructions executed by a digital signal processing device or other central processing unit, firmware, and/or hardware. The following are a brief description of terms referenced in Figure 4.

R_S = Transmission rate of the overhead channel (block 500B)

R_{EAV} = Available transmission rate for combination of the HDLC1 and HDLC2 channels

R_{HDLC1} = Minimum desired transmission rate for HDLC1 channel

R_{HDLC2} = Minimum desired transmission rate for HDLC2 channel

N_{HDLC1} = Number of bytes reserved for HDLC1 channel

N_{HDLC2} = Number of bytes reserved for HDLC2 channel

N_{EAV} = Number of bytes reserved for combination of HDLC1 and HDLC2 channels

N_{500} = Total number of bytes in MPS-TC frame

N_{CRC} = Number of bytes reserved for CRC

L_S = Number of bits per DMT symbols carrying bytes of the management/control information

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(All of the foregoing transmission rates are in kbps.)

The following is a relationship of terms referenced in Figure 4.

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$$R_{EAV} = R_S * (N_{EAV} / N_{500})$$

$$N_{HDLC1} = (R_{HDLC1} / R_{EAV}) * N_{EAV}$$

$$N_{HDLC2} = N_{EAV} - N_{HDLC1}$$

$$N_{EAV} = N_{500} - (N_{CRC} + 4)$$

15 **[0047]** In action 610, the transmitter determines the minimum desired bandwidth allocated for the combination of the HDLC1 and HDLC2 channels. Variables R_{HDLC1} and R_{HDLC2} represent the minimum desired transmission/rate of respective HDLC1 and HDLC2 channels.

20 **[0048]** Action 620 follows action 610. In action 620, the transmitter determines the available overhead bandwidth for the combination of the HDLC1 and HDLC2 channels (variable R_{EAV}).

25 **[0049]** Action 630 follows action 620. In action 630, the transmitter determines whether the available overhead bandwidth for the combination of the HDLC1 and HDLC2 channels (variable R_{EAV}) is greater than the combination of minimum transmission/bandwidth for HDLC1 and HDLC2 channels. If so action 640 follows action 630; otherwise action 670 follows action 630.

30 **[0050]** In action 640, the transmitter determines the number of bytes reserved for the HDLC1 channel (N_{HDLC1}). In one embodiment, the value N_{HDLC1} is determined by the following equation:

$$N_{HDLC1} = (R_{HDLC1} / R_{EAV}) * N_{EAV}$$

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If N_{HDLC1} is not an integer, it is rounded up to the nearest integer.

[0051] Action 650 follows action 640. In action 650, the transmitter determines the number of bytes reserved for the HDLC2 channel (variable N_{HDLC2}). In one embodiment the variable N_{HDLC2} is determined by the following equation:

$$N_{\text{HDLC2}} = N_{\text{EAV}} - N_{\text{HDLC1}}$$

[0052] Action 660 follows action 650. In action 660, the transmitter determines whether the available transmission rate for the HDLC2 channel is greater than or equal to the minimum desired transmission rate for the HDLC2 channel. In one embodiment, the following equation is a suitable representation of action 660:

$$\text{Is } R_{\text{EAV}} (N_{\text{HDLC2}} / N_{\text{EAV}}) \geq R_{\text{HDLC2}}$$

If so, then action 680 follows action 660; otherwise action 670 follows action 660.

[0053] In action 670, the transmitter increases the transmission rate of the overhead channel (block 500B) (value R_s) thereby to increase the transmission rate available for transmission of the HDLC2 channel. For example, the transmitter may increase the transmission rate of the overhead channel (block 500B) (value R_s) by 4 kbps. A maximum transmission rate (R_s) can be the maximum total link bandwidth capacity.

[0054] Action 680 follows action 660. In action 680, the transmitter determines the number of bits per DMT symbol (L_s) to transfer the block 500B of Figure 3C. Here R_s is assumed to be in kbps. For example, L_s can be determined by dividing R_s by the DMT symbol rate (e.g., 4 kbps).

[0055] Action 690 follows action 680. In action 690, the transmitter determines whether the number of bytes reserved for the HDLC1 channel (N_{HDLC1}) is greater than zero. If so, action 710 follows action 690; otherwise action 700 follows action 690.

[0056] In action 700, the transmitter assigns all EAV bytes (bytes reserved for the combination of HDLC1 and HDLC2) for use by HDLC2.

[0057] In action 710, the transmitter assigns, for example, N_{HDLC1} odd EAV bytes to HDLC1 and all other bytes to HDLC2.

[0058] The following is an example of results generated by Figure 4. For example, assuming

$$R_s = 68 \text{ kbps}$$

$$N_{500} = 68$$

$$N_{\text{CRC}} = 1$$

5 $R_{\text{HDLC1}} = 4 \text{ kbps}$

$$R_{\text{HDLC2}} = 59 \text{ kbps}$$

Then, in accordance with one embodiment of the present invention, the following values will be determined:

10

$$R_{\text{EAV}} = 63$$

$$N_{\text{HDLC1}} = 4$$

$$N_{\text{HDLC2}} = 59$$

$$N_{\text{EAV}} = 63$$

15

Thereby, in accordance with action 710 of Figure 4, the transmitter would assign EAV(1), EAV(3), EAV(5) and EAV(7) (Figure 3B) for use by HDLC1 and the rest of the overhead channel bytes of the EAV bytes to the HDLC2.

20 Modifications

[0059] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. For example, the transmission rate of the overhead channel (R_s) may vary or involve assigning even EAV bytes to HDLC1 and all other bytes to HDLC2. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

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CLAIMS

What is claimed is:

- 1 1. A method of allocating overhead within DMT ADSL frames, the method comprising
2 the acts of:
 - 3 allocating an interleaved data path;
 - 4 allocating a fast data path;
 - 5 allocating a path for overhead and management information independent of
6 the fast and interleaved data paths; and
 - 7 within a DMT ADSL frame, combining the overhead and management
8 information with the interleaved and fast data paths.
- 1 2. The method of Claim 1, wherein the overhead and management information
2 comprises interleaved data path related information.
- 1 3. The method of Claim 1, wherein the overhead and management information
2 comprises CRC bytes.
- 1 4. The method of Claim 1, wherein the overhead and management information
2 comprises IB bytes.
- 1 5. The method of Claim 1, wherein the overhead and management information
2 comprises aoc bytes.
- 1 6. The method of Claim 1, wherein the overhead and management information
2 comprises eoc bytes.
- 1 7. The method of Claim 1, wherein the overhead and management information
2 includes a first and second types of control information, wherein the bit rates of the first and
3 second types of control information are programmable.
- 1 8. The method of Claim 1 further comprising the acts of:
 - 2 determining a number of bytes allocable to first and second portions of the
3 overhead and management information; and
 - 4 allocating the number of bytes for the first and second portions within the
5 overhead and management information.
- 1 9. The method of Claim 8, wherein the act of determining a number of bytes further
2 comprises the acts of:

3 determining a minimum desired transmission rate for the combination of first
4 and second portions;
5 determining the available overhead bandwidth for the combination of first
6 and second portions; and
7 adjusting the available overhead bandwidth for the combination of first and
8 second portions to be at least the desired transmission rate for the combination of
9 first and second portions.

1 10. A method of allocating overhead within DMT ADSL frames, the method comprising
2 the acts of:

3 allocating an interleaved data path;
4 allocating first sync bytes among the interleaved data path;
5 allocating a fast data path;
6 allocating second sync bytes among the fast data path;
7 allocating a path for overhead and management information independent of
8 the fast and interleaved data paths; and
9 within a DMT ADSL frame, combining the overhead and management
10 information with the interleaved and fast data paths.

1 11. The method of Claim 10, wherein the first sync bytes includes overhead and
2 management information related to the interleaved path.

1 12. The method of Claim 10, wherein the second sync bytes includes overhead and
2 management information related to the fast path.

1 13. The method of Claim 10, wherein the overhead and management information
2 comprises CRC bytes.

1 14. The method of Claim 10, wherein the overhead and management information
2 comprises IB bytes.

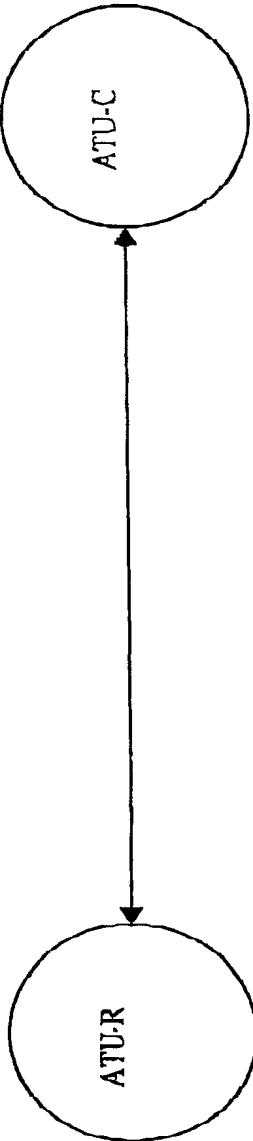
1 15. The method of Claim 10, wherein the overhead and management information
2 comprises aoc bytes.

1 16. The method of Claim 10, wherein the overhead and management information
2 comprises eoc bytes.

1 17. The method of Claim 10, wherein the overhead and management information
2 comprises a first and second types of control information, wherein the bit rates of the first
3 and second types of control information are programmable.

- 1 18. The method of Claim 10 further comprising the acts of:
2 determining a number of bytes allocable to first and second portions of the
3 overhead and management information; and
4 allocating the number of bytes for the first and second portions within the
5 overhead and management information.
- 1 19. The method of Claim 18, wherein the act of determining a number of bytes further
2 comprises the acts of:
3 determining a minimum desired transmission rate for the combination of first
4 and second portions;
5 determining the available overhead bandwidth for the combination of first
6 and second portions; and
7 adjusting the available overhead bandwidth for the combination of first and
8 second portions to be at least the desired transmission rate for the combination of
9 first and second portions.
10

Figure 1A



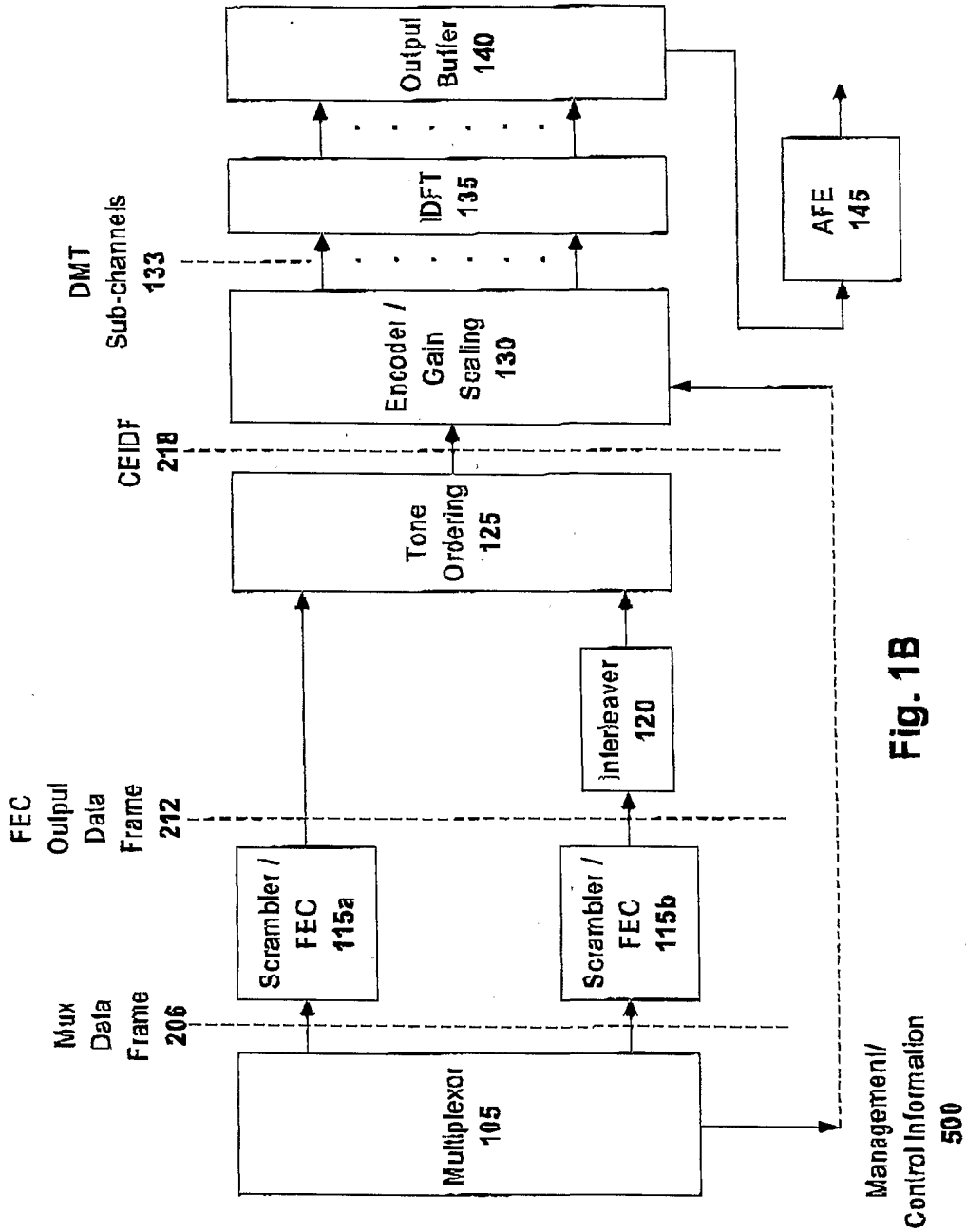


Fig. 1B

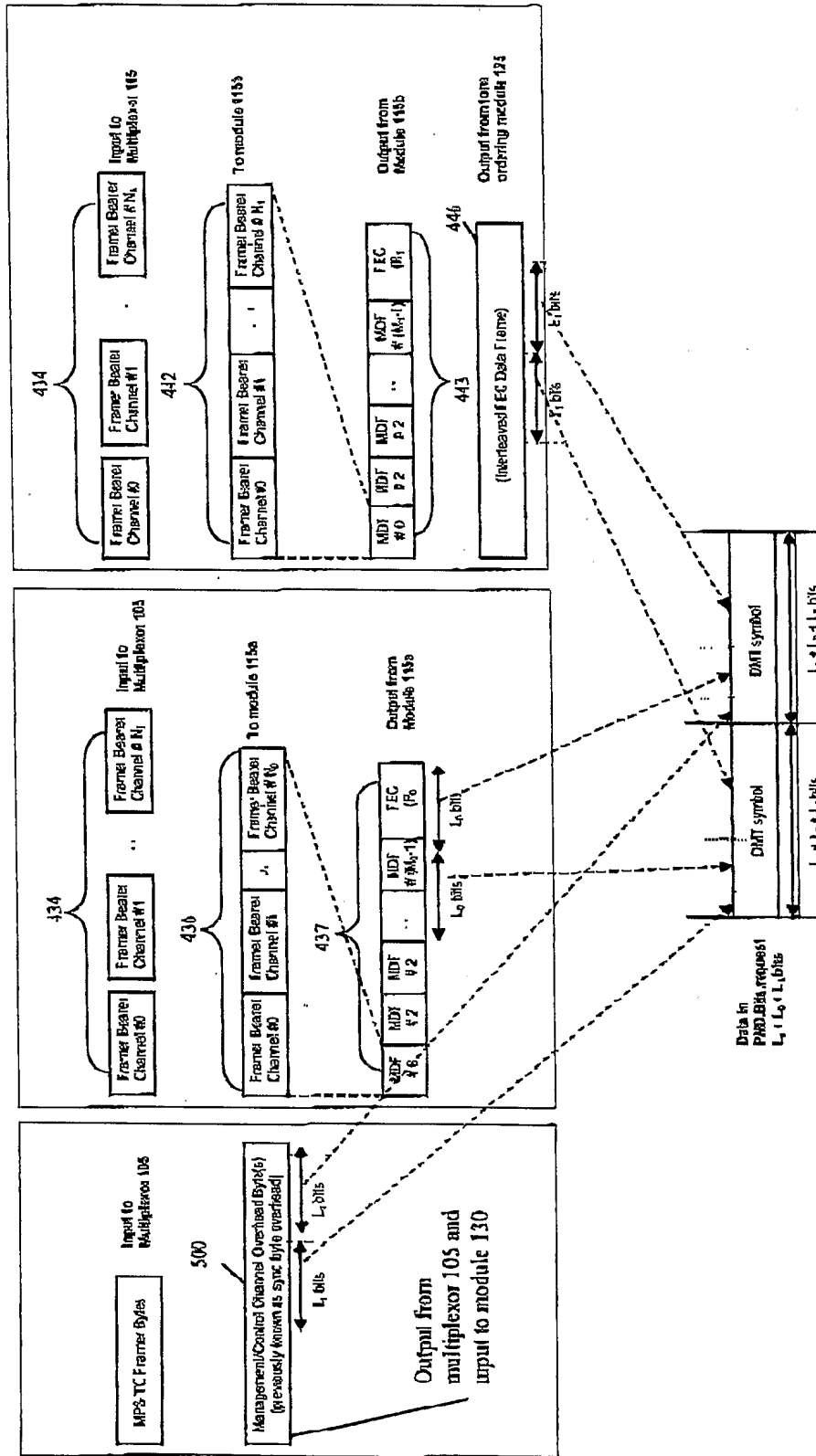
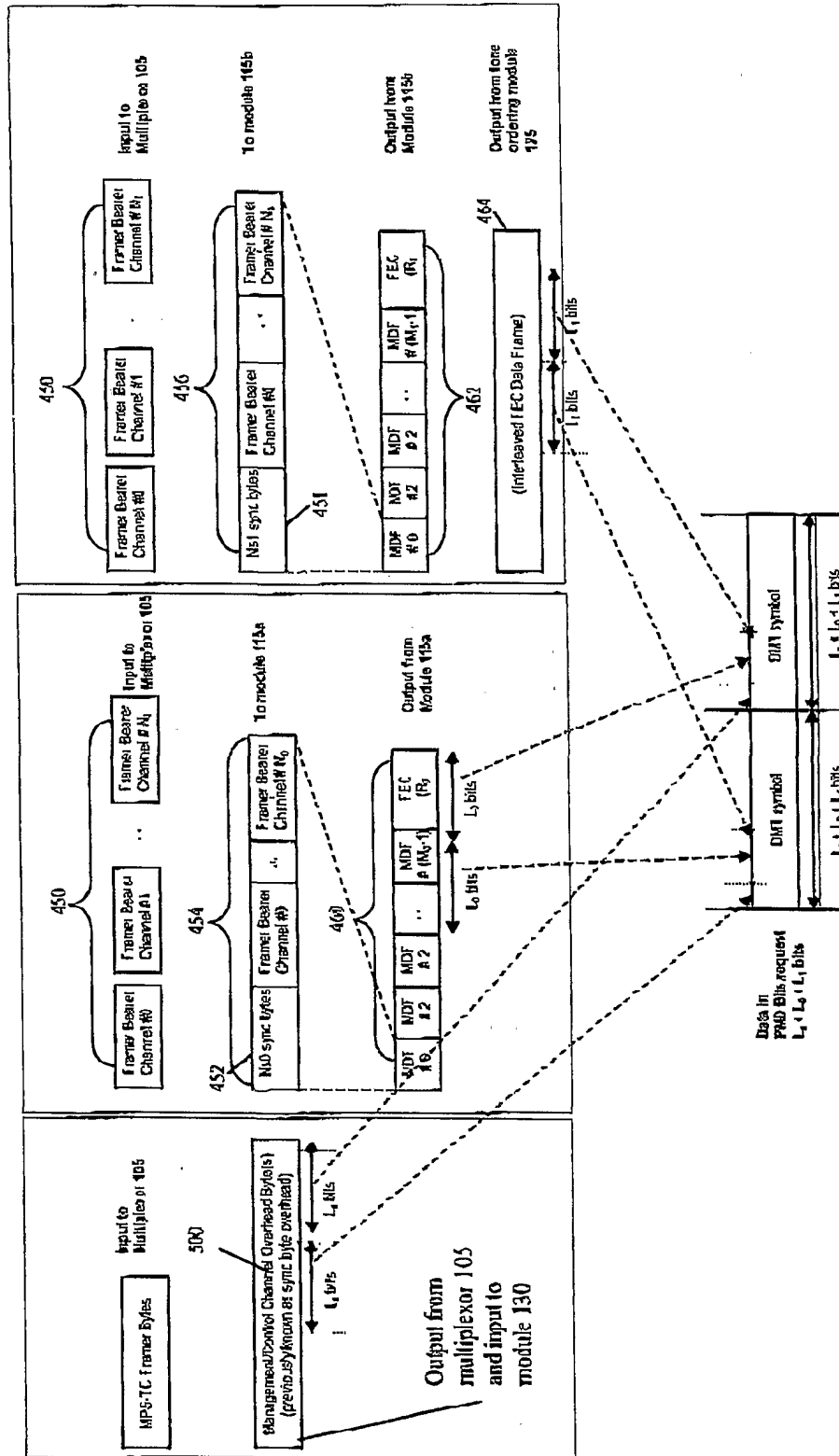


Figure 2A

Figure 2B



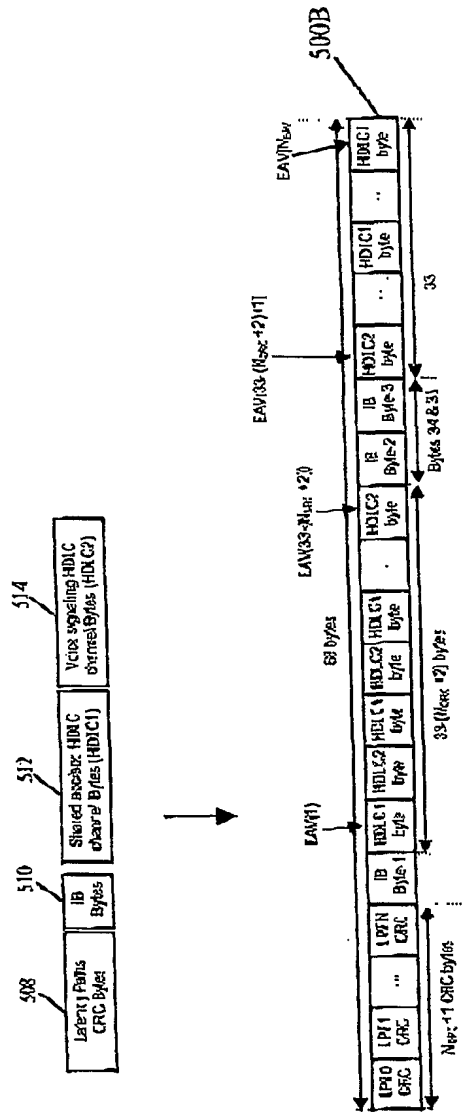


Figure 3B

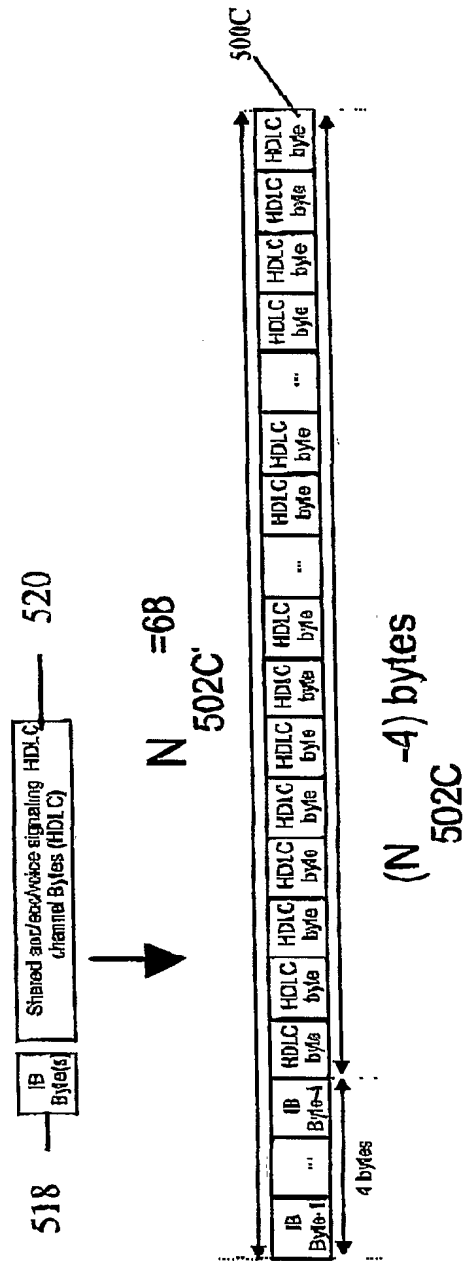


Figure 3C

Figure 4

